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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 3:08-cv-00877 PSG **DEFENDANTS' MOTION FOR RECONSIDERATION OF CERTAIN ASPECTS OF CLAIM CONSTRUCTION**

HTC CORPORATION and HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. 3:08-cv-00882 PSG
BARCO, N.V., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. 3:08-cv-05398 PSG

Introduction

In Judge Ware's First Claim Construction Order (Docket No. 336, June 12, 2012), the Court construed the term "separate direct memory access central processing unit" ("separate DMA CPU") to mean "a central processing unit that accesses memory and **that fetches and executes instructions** directly, separately, and independently of the main central processing unit." *See* Order at 11-13 (emphasis added). In doing so, the Court relied on portions of the written description to the effect an object of the claimed invention was a DMA that itself acted as a CPU. This led the Court to construe "separate DMA CPU" to mean what will be referred to herein as a "DMA co-processor" because, under the Court's construction, it fetches and executes instructions independently of the main CPU.

This Motion for Reconsideration is intended to bring to the Court's attention a previously unaddressed aspect of the prosecution history that sheds a new and different light on the Court's construction.[1] Specifically, early on in the prosecution of the Moore patent application, the USPTO issued a ten-way restriction requirement requiring the applicant to pursue ten different divisional applications stemming from the original application. Most relevant here, the USPTO restricted the DMA co-processor invention to a separate application that is *not* the application that resulted in the '890 patent. In other words, while the Court is correct that the specification describes, among other things, a DMA co-processor, *that* invention was pursued in a *different* application.

The application for the '890 patent was the subject of the restriction requirement. The '890 application was specifically restricted to a microprocessor *architecture* that includes a *conventional* DMA controller, and not the DMA co-processor. In light of that history, which is set out in detail below, TPL requests the Court reconsider its construction of the term "separate DMA CPU."

[1] Due to the 10 divisional applications and 16 reexaminations of the patents stemming from the original Moore application, the prosecution history for the entire patent family is in excess of several tens of thousands of pages.

Argument

I. THE ORIGINALLY FILED CLAIMS INCLUDED BOTH A DMA CO-PROCESSOR EMBODIMENT AND A CONVENTIONAL DMA CONTROLLER EMBODIMENT.

Defendants' Moore Microprocessor Patent ("MMP") Portfolio includes file histories covering thirty-seven (37) applications resulting in seven (7) issued U.S. patents. In addition, the Plaintiffs in the present cases and other parties have filed sixteen (16) reexamination requests in the U.S. Patent and Trademark Office, and a nullity action in the European Patent Office, that has greatly multiplied the volume of the file histories for the MMP Portfolio. In total, the MMP Portfolio file histories (including reexamination proceedings) comprise approximately 291 U.S. patent references, 33 foreign patent references, 382 non-patent references, 134 litigation-related pleadings or transcripts, and 205 office actions and responses, leading to over 30,000 pages of correspondence between the applicants and PTO and over 1,000 references. The '890 patent, as well as the other patents in suit, stemmed from a single application filed on August 3, 1989, which ultimately resulted in the MMP Portfolio.[2] That original application included 70 claims, disclosing a large number of independent and distinct inventions.

Claim 13 of the original application was specifically directed to the DMA co-processor invention:

> 13. A microprocessor system, comprising a central processing unit, a direct memory access processing unit, a memory, a bus connecting said central processing unit and said direct memory processing unit to said memory, said memory containing instructions for said central processing unit and said direct memory access processing unit, said **direct memory access processing unit including means** for fetching instructions for said central processing unit on said bus and **for fetching instructions for said direct memory processing unit** on said bus.

Much like the Court's construction of DMA CPU, originally-filed claim 13 required the DMA processing unit to fetch its own instructions.

[2] The original application, No. 07/389,334, eventually issued as U.S. Patent No. 5,440,749, one of the patents-in-suit.

By contrast, originally-filed claim 48 (which eventually became claim 1 of the '890 patent and later claim 11 of the reexamined '890 patent, the claim at-issue here) recited the use of a conventional DMA in a microprocessor architecture:

> A microprocessor, which comprises a main central processing unit **and a separate direct memory access central processing unit** in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said incrementer being connected to said internal data bus, said direct memory access central processing unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

Originally-filed claims 49-57 depended from this claim, and did not mention or modify the claimed DMA.

II. THE RESTRICTION REQUIREMENT.

Because the original application contained so many different inventions, the examiner imposed a remarkable *ten-way* restriction requirement on August 31, 1992.[3] The restriction requirement divided the disclosed inventions into ten categories as follows:

Group I, claims 1 and 2, "drawn to [a] microprocessor system having a multiplex bus, was filed as a divisional application on 07-Jun-95, US application number 08/480,462. That application was abandoned.

Group II, claims 3, 6-11, 26-30 and 32-47, "drawn to a processor system having means for fetching multiple instructions in parallel during a single machine cycle" (the description of the group given by the examiner), and were patented as US '749.

[3] See 35 U.S.C. § 121 ("If two or more independent and distinct inventions are claimed in one application, the Director may require the application to be restricted to one of the inventions.")

Group III, claim 13, "drawn to a microprocessor system having a DMA for fetching instruction[s] for a CPU and itself," was filed as a divisional application on 07-Jun-95 as patent application number 08/480,015. That application was abandoned.

Group IV, claims 16-18 and 63-64, "drawn to a processing system configured to provide different memory access time[s] for different amounts of memory," was filed on 07-Jun-95 as US application number 08/485,031. That application issued as US patent number 5,604,915 on 18-Feb-97.

Group V, claims 19-20 and 65-67, "drawn to [a] method and apparatus which operates as a variable clock speed," was filed on 07-Jun-95 as US application number 08/484,918. That application issued as US Pat number 5,809,336 on 15-Sep-98.

Group VI, claims 22-23, "drawn to a CPU having stacks and pointers," was filed on 07-Jun-95 as US patent application number 08/484, 230. That application was abandoned.

Group VII, claims 24-25 and 69-78, "drawn to a processing system for processing polynomial instruction[s]," was filed on 07-Jun-95 as US application number 08/484,720. That application was abandoned.

Group VIII, claims 48-57, "drawn to a microprocessor architecture," was filed on 07-Jun-95 as US patent application number 08/480, 206. That application issued as US patent number 5,530,890.

Group IX, claims 58-62, "drawn to method for prefetching," was filed on 07-Jun-95 as US patent application number 08/484,935. That application issued as US Pat number 5,784,584 on 21-Jul-98.

Group X, claim 68, "method for operating a stack," was filed on 07-Jun-95 as US application number 08/482,185. That application issued as US patent number 5,659,703 on 19-Aug-97.

SUMMARY OF RESTRICTION REQUIREMENT

I	II	**III**	IV	V	VI	VII	**VIII**	IX	X
micro-processor system having a multiplex bus	fetching multiple instructions in parallel during a single machine cycle	micro-processor system having a DMA for fetching instruction[s] for a CPU and itself	different memory access time[s] for different amounts of memory	method and apparatus which operates as a variable clock speed	CPU having stacks and pointers	system for processing polynomial instruction[s]	micro-processor architecture	method for prefetching	for operating a stack

Abandoned

'890 patent

Relevant here, the claims that eventually issued as the '890 patent were in Group VIII, and divided into application No. 08/480,206. Per the restriction requirement, those claims were "drawn to a microprocessor architecture." The '890 patent issued on a first action allowance (*i.e.*, as written, with no rejections).

Originally-filed claim 13, the DMA co-processor invention, was in Group III, constituting inventions "drawn to a microprocessor system having a DMA for fetching instruction[s] for a CPU and itself." The Group III application, No. 08/480,015, was eventually abandoned.

This prosecution history demonstrates that there were two separate DMA inventions in the original application: (1) a microprocessor architecture with conventional DMA controller, and (2) a DMA co-processor. These two inventions were prosecuted separately, and invention (1) issued as the '890 patent. The objects of invention language relied upon by the Court for its construction was directed to the DMA co-processor claimed in originally filed claim 13, and not the microprocessor architecture invention claimed in the '890 patent. Therefore, the Court should reconsider its construction of "separate direct memory access central processing unit."

III. THE REEXAMINATION PROCEEDINGS CONFIRM THAT DMA CPU MEANS A CONVENTIONAL DMA CONTROLLER.

The '890 patent was reexamined. Although claim 11, the claim under construction, was added during reexamination, it varies from pre-reexamination claim 1 only in that "said stack pointer pointing to said first push down stack" was added. Nothing about the DMA CPU was changed.

The consistent meaning of the claim term "a separate direct memory access central procession unit," used by the reexamination requester, the USPTO, and the applicant, is a conventional DMA controller.

For example, in the reexamination request filed by Fish & Richardson, the requestor argued:

> The **'890 patent teaches a direct memory access controller** and states that "conventional microprocessors provide direct memory access (DMA) for system peripheral units through DMA controllers, which may be located on the microprocessor integrated circuit" (Id., 1:52-55)

Ex Parte Request for Reexamination, at 8. The requestor further argued:

> … Requestor submits that the **DMA controllers were conventionally placed on the same chip as of the '890 patent's priority date** and thus this feature would have been considered obvious by one of ordinary skill in the art. For example, US patent number 4,783,764 to **Tsuchiya** et al. **describes** a **Direct Memory Access Controller** on a single integrated circuit with a CPU….

Id., at 11 (describing the "mode exchange circuit 9" shown in Tsuchiya, FIG. 3 as a DMA controller).

The USPTO granted the reexamination request on April 8, 2009, in an order stating:

> … **Tsuchiya** describes a microprocessor further including a separate **direct memory access central processing unit**…

Order Granting Ex Parte Reexamination, at 7. In the first action on the merits, dated 05-Nov-09, the examiner stated:

> … [T]he "Transputer Manual" … is seen to describe an **on-chip DMA controller**….

PTO Non-Final Office Action, at 4. Further, the Examiner went on to note:

> … [T]he references cited in the request for re-examination on page 11 (as well is pages 26 and 27) that teach of an **on-chip DMA controllers**…

Id.

These excerpts confirm that during reexamination, the patent owner and the USPTO considered the DMA controller of the '890 patent to be a conventional DMA controller and not a DMA co-processor, capable of fetching and executing instructions. At no time did the patent owner ever try to distinguish the prior art on the ground that the '890 patent required a DMA co-processor, even though that would have been an obvious basis for distinction if true.

Conclusion

TPL's originally proffered claim construction of the term – "electrical circuit for reading and writing to memory that is separate from a main CPU" – was correct in that it does not limit the construction of DMA CPU to only one of the two disclosed microprocessor architecture embodiments (Figs. 2 and 9). The Court's construction limiting the DMA CPU to the DMA co-processor embodiment is incorrect in light of the prosecution history. It is clear from the prosecution history that the patentee, the USPTO, and even the reexamination requestor, all understood that a DMA CPU encompasses a conventional DMA. Therefore, reconsideration is requested.

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Respectfully submitted,

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